REMARKS

Claims 1-31 are pending in the present application. Claims 1, 21 and 23 are independent claims. Claims 1, 21 and 23 are amended by this Reply. Reconsideration of this application, as amended, is respectfully requested.

REJECTIONS UNDER 35 U.S.C. §102

Claims 1-4, 7-11, 13-14, 16-19, 21-25 and 27-31 stand rejected under 35 U.S.C. §102(e) over U.S. Patent No. 6,411,346B1 to Numano et al. (Numano), for the reasons set forth in paragraph 1 of the Office Action. This rejection is respectfully traversed.

A feature of the Applicants' claimed invention is a metallic pattern for forming a drain electrode and an upper electrode of a storage capacitor, formed along a periphery of one cell in order to surround the cell.

Numano discloses a liquid crystal display comprising a plurality of gate lines and data lines, thin film transistors, storage capacitor, and in particular, a drain electrode of a thin film transistor and an upper electrode of the storage capacitor formed with a consecutive pattern (see Fig.14). The storage capacitor of Numano is formed by additional storage wiring 3 that is formed within one pixel cell area, i.e., crossing the central portion of the cell, and the upper electrode formed over the storage wiring 3 (see at least Figs 1, 6 and 9).

By contrast, the metallic pattern of the Applicants' claimed invention is formed along a periphery of one cell in order to surround the cell. Further, the storage capacitor of the Applicants' claimed invention comprises an upper

electrode of the storage capacitor and one of the gate lines. Therefore, the rejection under 35 U.S.C. 102 is not proper.

In particular, Numano fails to teach a storage capacitor, surrounding the cell, including a storage electrode and a drain electrode in a single layer, the storage capacitor being connected to the pixel electrode, wherein the storage electrode is formed over the one of the gate lines, as recited in independent claim 1, as amended, and similarly stated in independent claim 21, as amended. Further, Numano fails to teach simultaneously forming a data line having a source electrode, and a metallic pattern including a drain electrode part and a storage electrode part in a single layer, wherein the storage electrode part is formed over the gate line, as recite in independent claim 23, as amended.

Claims 2-4, 7-11, 13-14, 16-19, 22, 24, 25 and 27-31depend, either directly or indirectly on independent claims 1, 21 and 23, and therefore are patentable at least for the reasons stated with respect to independent claims 1, 21 and 23. Reconsideration and withdrawal of this art grounds of rejection are respectfully requested.

REJECTIONS UNDER 35 U.S.C. §103

Claims 5-6, 12, 15, 20 and 26 stand rejected under 35 U.S.C. §103(a) over Numano as applied to claims 1, 21 and 23, in view of U.S. Patent No. 5,995,175A to Kim. This rejection is respectfully traversed.

Numano, argued above with respect to claims 1, 21 and 23, fails to disclose or suggest a storage capacitor, surrounding the cell, including a storage electrode

and a drain electrode in a single layer, the storage capacitor being connected to the pixel electrode, wherein the storage electrode is formed over the one of the gate lines, as recited in independent claim 1, as amended, and similarly stated in independent claim 21, as amended. Further, Numano fails to disclose or suggest simultaneously forming a data line having a source electrode, and a metallic pattern including a drain electrode part and a storage electrode part in a single layer, wherein the storage electrode part is formed over the gate line, as recite in independent claim 23, as amended . Kim cannot fill this vacancy.

Claims 5-6, 12, 15, 20 and 26 depend, either directly or indirectly, on independent claims 1, 21 and 23. Since neither Numano, nor Kim discloses or suggests the above-recited features of independent claims 1, 21 and 23, Numano, in view of Kim cannot render claims 5-6, 12, 15, 20 and 26 obvious to one of ordinary skill in the art. Reconsideration and withdrawal of this art grounds of rejection are respectfully requested.

CONCLUSION

Applicants point out that all of the Examiner's comments have been addressed and that all of the Examiner's objections and rejections have been overcome, thereby placing all claims pending in the present Application in condition for allowance. Allowance of the claims is respectfully solicited.

In the event that any outstanding matters remain in this application, Applicants request that the Examiner contact Percy L. Square at (703) 205-8034 to discuss such matters.

Attached hereto is a marked-up version of the changes made to the application by this Amendment.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2448 for any additional fees required under 37 C.F.R. §§ 1.16 or 1.17; particularly, extension of time fees.

Respectfully submitted,

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Attachment: Version with Markings to Show Changes Made

(Rev. 02/06/01)

VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS:

The claims have been amended as follows:

1. (Three Times Amended) A liquid crystal device having a thin film transistor, comprising:

a plurality of gate lines formed on a substrate;

a plurality of data lines insulated from and intersecting said gate lines, said data lines and intersecting gate lines defining a plurality of cells, at least one cell including,

a pixel electrode,

a thin film transistor connected to one of the data lines and one of the gate lines defining the cell,

a storage capacitor, and

a metallic pattern, surrounding the cell, including a drain electrode of the thin film transistor and a storage electrode of the storage capacitor in a single layer and being electrically connected to the pixel electrode, wherein the storage electrode is formed over the one of the gate lines.

21. (Three Times Amended) A liquid crystal device having a thin film transistor, comprising:

a plurality of gate lines formed on a substrate;

a plurality of data lines insulated from and intersecting said gate lines, said data lines and intersecting gate lines defining a plurality of cells, at least one cell including,

a pixel electrode,

a thin film transistor interposed between one of the data lines and the pixel electrode and including a source electrode connected to the one of the data lines, a gate electrode connected to one of the gate lines, a drain electrode, and

a storage capacitor, surrounding the cell, including a storage electrode and a drain electrode in a single layer, the storage capacitor being connected to the pixel electrode, wherein the storage electrode is formed over the one of the gate lines.

23. (Three Times Amended) A method of manufacturing a thin film transistor substrate, comprising:

forming a gate line having a gate electrode on a transparent substrate;

forming a gate insulating layer on the gate electrode;

forming a semiconductor layer on the gate insulating layer;

simultaneously forming a data line having a source electrode, and a metallic pattern including a drain electrode part and a storage electrode part in a single layer, wherein the storage electrode part is formed over the gate line;

[forming a semiconductor layer over at least a portion of one of the gate electrodes, at least a portion of one of the source electrodes, and at least a portion of the drain electrode part in a single layer;]

forming a protective film over the entire surface; and

forming a pixel electrode over the protective film.